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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/677,257	10/03/2003	Satoshi Inoue	039282.03	9107
25944	7590	11/02/2005	EXAMINER	
OLIFF & BERRIDGE, PLC P.O. BOX 19928 ALEXANDRIA, VA 22320			TRINH, MICHAEL MANH	
			ART UNIT	PAPER NUMBER
			2822	

DATE MAILED: 11/02/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

EL

Office Action Summary	Application No.	Applicant(s)	
	10/677,257	INOUE, SATOSHI	
	Examiner	Art Unit	
	Michael Trinh	2822	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

- 1) ☒ Responsive to communication(s) filed on 15 August 2005.
- 2a) ☒ This action is **FINAL**. 2b) ☐ This action is non-final.
- 3) ☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

- 4) ☒ Claim(s) 8,9 and 15-32 is/are pending in the application.
- 4a) Of the above claim(s) 21 and 23-29 is/are withdrawn from consideration.
- 5) ☐ Claim(s) _____ is/are allowed.
- 6) ☒ Claim(s) 8,9,15-20,22 and 30-32 is/are rejected.
- 7) ☐ Claim(s) _____ is/are objected to.
- 8) ☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

- 9) ☐ The specification is objected to by the Examiner.
- 10) ☐ The drawing(s) filed on _____ is/are: a) ☐ accepted or b) ☐ objected to by the Examiner.
Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).
Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).
- 11) ☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

- 12) ☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
- a) ☐ All b) ☐ Some * c) ☐ None of:
1. ☐ Certified copies of the priority documents have been received.
2. ☐ Certified copies of the priority documents have been received in Application No. _____.
3. ☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

- | | |
|---|---|
| 1) <input checked="" type="checkbox"/> Notice of References Cited (PTO-892) | 4) <input type="checkbox"/> Interview Summary (PTO-413) |
| 2) <input type="checkbox"/> Notice of Draftsperson's Patent Drawing Review (PTO-948) | Paper No(s)/Mail Date. _____ |
| 3) <input type="checkbox"/> Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) | 5) <input type="checkbox"/> Notice of Informal Patent Application (PTO-152) |
| Paper No(s)/Mail Date _____ | 6) <input type="checkbox"/> Other: _____ |

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DETAILED ACTION

*** This office action is in response to Applicant's Amendment filed on August 15, 2005.

Claims 8-9,15-32 are pending.

*** The text of those sections of Title 35, U.S. Code not included in this action can be found in a prior Office action.

Election/Restrictions

1. Newly submitted claims 21,23-29 (e.g. Figs 4A,5-6) are directed to an invention that is distinct from the invention originally claimed in original elected claims 8-9,15-20,22,30-32 (e.g. Figs 1-3) for the following reasons: New claim 21,23-29 are directed to another embodiment, in which forming a third region including a first part being located between the first region and the channel region and a second part located between the second region and the channel region (e.g. Figs 4A,5-6). Since applicant has received an action on the merits for the originally presented invention of subject matter of original elected claims, in which base claim 8 at least includes a plurality of third regions and located between the first and second regions, claims 21,23-29 have been constructively elected by original presentation and examination for prosecution on the merits.

Accordingly, new claims 21,23-29 are withdrawn from consideration as being directed to a non-elected invention. See 37 CFR 1.142(b) and MPEP § 821.03.

2. This application contains claims 21,23-29 drawn to an invention nonelected in this office action. A complete reply to the final rejection must include cancellation of nonelected claims or other appropriate action (37 CFR 1.144) See MPEP § 821.01.

Claim Rejections - 35 USC § 112

1. Claims 31-32 are rejected under 35 U.S.C. 112, first paragraph, as containing subject matter which was not described in the specification in such a way as to reasonably convey to one skilled in the relevant art that the inventor(s), at the time the application was filed, had possession of the claimed invention.

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Re claim 31-32, original specification does not support "...first end of the first region and the first end of the second region having a width more narrow than a width of the plurality of third regions (claim 31); and in claim 32, "...the width of the plurality of third regions being about 20mm larger than the width of either of the first end..." (claim 32).

As can be seen in Figure 1A, original specification differently teaches the first end of the first region 17 having a width wider than a width of each of the plurality of third regions 23. Especially, nowhere in the specification mention "20mm" of claim 32, in which the width of the plurality of third regions is being about 20mm larger than the width of either of the first ends.

Claim Rejections - 35 USC § 102

2. Claims 8,9,22,30 are rejected under 35 U.S.C. 102(b) as being anticipated by Nakagawa et al (5,477,065).

Re claim 8, Nakagawa teaches a method for forming a transistor comprising: forming a semiconductor film on the substrate (e.g. Figs 22A-23B; col 12, lines 22-46; and col 11, line 10 through col 12; Fig 17-21,17-19C); forming a plurality of third region (203 in Figs 22A,22B, 23A,23B; 102 in Figs 19A,19C,17) in the semiconductor film by a first ion doping of a second conductivity type, each of the plurality of third regions being separated by a space; forming an insulator film 205 (104 in Figs 19A-19C) over the semiconductor film; forming a gate electrode 206 (105 in Figs 19A-19C) over the insulator film 205 (Figs 22A,23A); and forming a first region (108 in Figs 19A-19C; in Figs 22A,22B, the p-region under the electrode 207 and adjacent the third regions 203) and a second region (e.g. 204 in Figs. 22A,22B,23A,23B; 103 in Figs 19A-19C) in the semiconductor film by a second ion doping of a second impurity of a first conductivity type, the gate electrode 206 overlapping at least a part of each of the plurality of the third regions 203 (Figs 22A,22B,23A, 23B), and the plurality of third regions located between the first region and the second region 204 (Figs 22A,22B,23A,23B). Re claim 9, wherein the semiconductor film having a channel region 201 under the gate electrode 206, the channel region 201 not including any of the first impurity of the second conductivity type in the third regions 203 and the second impurity of a first conductivity type of the second region 204 (Figs 22A,22B,23A,23B). Re claim 22, wherein the dosage of the second impurity of the first and second regions (102/103 in Figs 17, 19A-19C; 204 in Figs 22-23) being smaller than a dosage of

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the first impurity of the third region (102 in Figs 17, 19A-19C; and 203 in Figs 22A,22B,23A,23B). Re claim 30, wherein the first region (108 in Figs 19C; and region under the electrode 207 in Figs 22-23) having a first end and a second end in opposite sides of the first region, the first end of the first region being in a side opposite the plurality of third regions, the second region (204 in Figs 22B,23B; 103 in Fig 19C) having a first end and a second end in opposites sides of the second region, the first end of the second region being in a side opposite the plurality of third regions (203 in Figs 22B,23B; 102 in 19C).

3. Claims 8,9,16,30 are rejected under 35 U.S.C. 102(b) as being anticipated by Okada (5,294,824).

Re claim 8, Okada teaches a method for forming a transistor comprising: forming a semiconductor film on the substrate (Figs 1-2; col 2, lines 44 through col 6); forming a plurality of third region 17 in the semiconductor film by a first ion doping of a second conductivity type, each of the plurality of third regions being separated by a space (Figs 1-2; col 3, line 62 through col 4; col 6, lines 17-29); forming an insulator film 27 over the semiconductor film; forming a gate electrode 13 over the insulator film (col 5, lines 1-41); and forming a first region 12 and a second region 14 in the semiconductor film by a second ion doping of a second impurity of a first conductivity type (col 4, lines 5-35; col 5, line 20 through col 6, lines 58), the gate electrode 13 overlapping at least a part of each of the plurality of the third regions 17 (Figs 1-2) and the plurality of third regions 17 located between the first region 12 and the second region 14.

Re claim 9, wherein the semiconductor film having a channel region 19 under the gate electrode 13, the channel region 19 not including any of the first impurity of the second conductivity type in the third regions 17 and the second impurity of a first conductivity type of the first and second regions 12/14 (Figs 1-2). Re claim 16, wherein the method further comprises forming a source electrode 29 and a drain electrode 32, the source electrode 29 being connected to the first region 12 underlying the source electrode, the drain electrode 32 being connected to the second region 14, and none of the source and the drain electrode being connected to the plurality of the third region 17 (Fig 1). Re claim 30, wherein the first region 12 having a first end and a second end in opposite sides of the first region, the first end of the first region being in a side opposite the plurality of third regions 17, the second region 14 having a first end and a second end in

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opposite sides of the second region, the first end of the second region being on a side opposite the plurality of third regions 17 (Figs 2,1).

Claim Rejections - 35 USC § 103

4. Claims 17-20 are rejected under 35 U.S.C. 103(a) as being unpatentable over either Nakagawa et al (5,477,065) or Okada (5,294,824, taken with Kawashima et al (5,016,986).

Nakagawa teaches a method for forming a transistor as applied to claims 8,9,22,30 above. Okada also teaches a method for forming a transistor as applied to claim 8 above.

Re claims 17-20, Nakagawa or Okada already teaches the method of manufacturing the transistor, but lacks using the method for manufacturing an active matrix substrate (claim 17), an electroluminescent device (claim 18), display device (claim 19), and an electronic apparatus (claim 20).

However, Kawashima teaches (at col 10, lines 60-68) applying the method in manufacturing a liquid crystal display as active matrix substrate (claim 17) and other devices including a plasma display device (re claim 19), an electroluminescence display device (claim 18), and electronic devices (claim 20).

Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to employ the method of manufacturing the transistor of Nakagawa or Okada in manufacturing other devices including the active matrix substrate as liquid crystal display, the electroluminescence display device, the plasma display device, and the electronic devices, as taught by Kawashima. This is because of the desirability to manufacture different and various types of devices by using transistors having high speed operation with lower power consumption.

5. Claim 15 is rejected under 35 U.S.C. 103(a) as being unpatentable over either Nakagawa et al (5,477,065) or Okada (5,294,824, taken with Kawashima et al (5,016,986).

Nakagawa teaches a method for forming a transistor as applied to claims 8,9,22,30 above. Okada also teaches a method for forming a transistor as applied to claim 8 above.

Re claim 15, Nakagawa or Okada already teaches forming a semiconductor film, but lacks applying an energy to crystallize the semiconductor film before forming the second region.

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However, Yamazaki teaches (at col 7, lines 52-67; Fig 7A; col 8, lines 1-26) applying an energy to crystallize the semiconductor film before forming the second regions 34a,34b (Fig &C,7D col 8, lines 59-67).

Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to employ the method of manufacturing the transistor of Nakagawa or Okada by applying an energy to crystallize the semiconductor film before forming the second region as taught by Yamazaki. This is because of the desirability to crystallize the semiconductor film by performing a heat treatment in order to form the crystallized semiconductor film having a desired carrier mobility.

Response to Amendment

6. Applicant's remarks filed August 15, 2005 have been fully considered but they are moot in view of the new ground(s) of rejection.

Applicant's amendment necessitated the new ground(s) of rejection presented in this Office action. Accordingly, **THIS ACTION IS MADE FINAL**. See MPEP § 706.07(a). Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).


A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the date of this final action.

*** Any inquiry concerning this communication or earlier communications from the examiner should be directed to Michael M. Trinh whose telephone number is (571) 272- 1847. The examiner can normally be reached on M-F: 8:30 Am to 5:00 Pm.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Amir Zarabian can be reached on (571) 272-1852. The fax phone number is (571) 273-8300

Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the receptionist whose telephone number is (703) 308-0956.

Oacs-16


Michael Trinh
Primary Examiner